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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/816,518 | 03/26/2001 | Hiroshige Goto | 205142US2S | 8020 |

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| EXAMINER | |
|---|---|
| TILLERY, RASHAWN N | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2612 | 7 |

DATE MAILED: 08/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/816,518 | GOTO, HIROSHIGE | |
| | Examiner | Art Unit | |
| | Rashawn N Tillery | 2612 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4 and 10* is/are allowed.

6)☒ Claim(s) *5-9,11 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2,4,5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-9 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al (US6674470) in view of Mizoguchi et al (US6512545).

Regarding claims 5 and 11, Takaka discloses, in figures 3 and 7, a solid-state imaging device comprising:

an imaging area having unit cells (30) arranged in a two-dimensional fashion on a semiconductor substrate, each of the unit cells including a photoelectric conversion/storage section (92a, 92b) for photoelectrically converting incident light and storing charges thus generated, a charge readout circuit (93a, 93b) for transferring charges stored in the photoelectric conversion/storage section to a charge detecting section (98), a potential detecting circuit (94) for detecting charges transferred to the charge detecting section, generating a potential corresponding to an amount of detected charges and transmitting the potential to a corresponding one of vertical signal lines (34), a reset circuit (96) for discharging the charges transferred to the charge detecting section, and an address circuit (95) for selectively activating the potential detecting circuit (see col. 7, line 36 to col. 8, line 44);

a vertical driving circuit (32) provided in correspondence to each pixel row of the imaging area, for driving the charge readout circuit, reset circuit and address circuit of each of the unit cells at preset timings;

signal processing circuits (48, 50, 54, 56, 58, 60) respectively attached to the vertical signal lines which are provided for respective columns of the unit cells, for performing required signal processes;

horizontal readout switching circuits (62) for controlling transfer of outputs of the signal processing circuits corresponding to the respective vertical signal lines to a horizontal signal line;

a horizontal driving circuit (68) for controlling the horizontal readout switching circuits at preset timings and

an output circuit (64) for outputting output signals of the signal processing circuits which are read out to the horizontal signal line by controlling the horizontal readout switching circuits by use of the horizontal driving circuit;

wherein the solid-state imaging device has a first operation mode in which the horizontal driving circuit sequentially turns ON the horizontal readout switching circuits in correspondence to the vertical signal lines to sequentially output the output signals of the signal processing circuits corresponding to the vertical signal lines from the output circuit via the horizontal signal line (Tanaka sequentially turns on H address 62-1 and 62-2 in figure 8).

Tanaka does not expressly disclose a second operation mode where the horizontal driving circuit turns ON the horizontal readout switching circuits at

substantially the same time to read out the output signals of the signal processing circuits.

Mizoguchi teaches a solid-state image apparatus for reading pixel signals out at a high frame rate. Mizoguchi reveals in one embodiment that it is well known in the art to concurrently drive output pulses to read out signals as they are added together (see col. 7, lines 18-51; also see col. 15, lines 18-46; also see figure 7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tanaka's device by implementing Mizoguchi's teachings since Mizoguchi reveals the added advantage of outputting high-definition images at higher frame rates.

Regarding claim 6, Tanaka discloses a horizontal address circuit for controlling pixel readout in Applicant's claimed first operation mode. Tanaka does not expressly disclose a pixel column selection information processing circuit or a pixel column selection circuit for switching between a first and second operation mode. Mizoguchi discloses, in figure 3, a pixel column selection information processing circuit (1) supplied with a signal (SIG) for selecting a pixel column, for decoding the signal for selecting a pixel column; and a pixel column selection circuit (6) supplied with a decoded output of the pixel column selection information processing circuit, for making switching between the first and second operation modes by controlling the horizontal driving circuit to output pulses at different timings in the first and second operation modes. Mizoguchi's device is operable in three modes- in one mode the output signal of the shift register is selectively outputted for a thinned-out readout; in a second mode the output signal of the shift register is concurrently outputted for an adder readout; and in a third the output

of the shift register is sequentially outputted for a sequential readout. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tanaka's device by implementing Mizoguchi's teachings since Mizoguchi reveals the added advantage of outputting high-definition images at higher frame rates.

Regarding claim 7, Tanaka discloses, in figure 8, the horizontal driving circuit includes a pulse generating section for outputting a horizontal readout pulse (62) and clear pulse (GATE 69 OF TR 60).

Regarding claims 8 and 12, Tanaka discloses, in figure 3, the horizontal readout switching circuits (62) include a group of transistors which are supplied with the outputs of the signal processing circuits (48, 50, 54, 56, 58, 60) corresponding to the vertical signal lines at one-side ends of current paths thereof and commonly connected to the horizontal signal line at the other ends of the current paths thereof and whose gates are supplied with the output signal of the horizontal driving circuit, the transistors being sequentially turned ON in the first operation mode and a plurality of transistors among the group of transistors being turned ON at substantially the same time in the second operation mode.

Regarding claim 9, Tanaka discloses each of the signal processing circuits includes a noise canceller circuit (see col. 8, line 45 to col. 9, line 35).

***Allowable Subject Matter***

Claims 1-4 and 10 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 1 and 10, the prior art does not teach or fairly suggest a solid-state imaging device comprising an imaging area having unit cells, each of the unit cells including first and second photoelectric conversion/storage section, a charge readout circuit, a potential detecting circuit, a reset circuit, an address circuit, a vertical driving circuit, signal processing circuits, a horizontal driving circuit and an output circuit, wherein

the device has a first operation mode in which the first and second charge readout circuits are driven at substantially the same timing by the vertical driving circuit, and the charges of the first and second photoelectric conversion/storage section are added together in the charge detecting section.

***Conclusion***

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Merrill teaches a triple slope pixel sensor array. Guidash teaches an APS with multiple photodiodes in a unit cell. Nomoto teaches an imager for selectively accessing pixel rows and columns. Matsunaga et al teach an imager with

multiple photodiodes in a cell. Wilder et al teach imager for selectively accessing pixel rows and columns. Nakamura et al teach an imager for selectively accessing pixel rows and columns.

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rashawn N Tillery whose telephone number is 703-305-0627. The examiner can normally be reached on 9AM-6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on 703-305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RNT

AUNG MOE
PRIMARY EXAMINER